Óbuda University Kandó Kálmán Faculty of Electrical Engineering		Department of Instrumentation ans Automation		
Subject name and code: Information Systems KMWIN5ABNE Credits: 3				
Specializations: Electrical Engineering				
Subject leader:		Teachers :	Borsos Döniz, Sándor Tamás	
Prerequisites: KMWAG2TBNA				
Lectures:	**Theory: 2**	**Seminar.: 0**	**Lab. Exec.: 1**	**Consultations: 0**
demands :	Exam			

Education material

Aim of education:

Topics:	**Week:**	
FPGA basics	**1.**	
FPGA, testwork: Logic design with simulation + theory	**2.**	
FPGA, ChipScope Pro virtual instruments (more details only ILA), use of IPs, instrumentation with logic analyzer	**3.**	
FPGA, FSM, Moore and Mealy models, status coding, high-level description of state machine: 7-segment display controller design, ChipScope Pro VIO: testing of a 7-segment display controller on Nexys4	**4.**	
SoC / SoPC, processors, SoC buses, HW / SW co-design	**5.**	
SoC / SoPC, IP generation and packaging	**6.**	
SoC / SoPC, MicroBlaze-based system design with Vivado: basic system with Block Design, Level 0 test with XMD, BSP + first application (hello world), Low-level and high-level drivers via GPIO peripheral example	**7.**	
SoC / SoPC, Adapting your own peripherals to the MicroBlaze-based system, Buses, SerDes	**8.**	
SoC / SoPC, SW, Software development project, control tasks	**9.**	
SW, CM, quality models and methodologies (Waterfall model, V-model, agile development / Scrum, Spice, CMMI)	**10.**	
SW, Claims Management and Tooling	**11.**	
SW, Testing and using metrics	**12.**	
Testwork and assignment	**13.**	
Assignment	**14.**	

Demand of the semester

The code to be created jointly (with the instructor) and independently in the laboratory exercise must be uploaded by everyone in the Google classroom created for the subject, which must be accompanied by documentation. Homework assignments issued in labs must be uploaded to the Google classroom in the same way on time. During the semester, 1 large electronic ZH thesis is expected and 1 large homework assignment. During the semester assignments and dissertations, the student must achieve at least 50% of everything in order to successfully complete the semester. Method of replacement Replacement is possible at the end of the semester, once.

Method of creating the exam mark: 25% of the exam mark is given by the average of the results of the control tests, homework and reports, 25% by the ZH dissertation, and 50% by the independent task. 0-50% insufficient, 51-65% sufficient, 66-75% medium, 76-90% good, 91-100% excellent

Literature:

FPGA F4modul.com/FPGA/Presentation 1a, 1b, 1c, 1d slide shows.
Books:
1. Pong P. Chu - FPGA Prototyping by VHDL Examples
2. Richard E. Haskell, Darrin M. Hanna - Digital Design Using Digilent FPGA Boards - VHDL / Active-HDL Edition
3. Enoch O. Hwang - Digital Logic and Microprocessor Design With VHDL
4. Peter J. Ashenden - The VHDL Cookbook Constraint file (nexys4_master.xdc): https://reference.digilentinc.com/reference/programmable-logic/nexys-4/start
Nexys 4 board files: https://reference.digilentinc.com/learn/software/tutorials/vivado-board-files/start