

Óbudai Egyetem Kandó Kálmán Villamosmérnöki Kar		Műszertechnikai és Automatizálási Intézet		
Course name and code: Safety critical software development KMWBS5TANE				
<i>Credits: 3</i>				
Specializations in which the subject is taught: <i>Villamosmérnök, KVK,</i>				
Subject leader:		Oktatók: Dr. Schuster György, Sándor Tamás, Borsos Döníz		
Prerequisites: (code)		-		
Hours per week:	Theory: 1	Practice.: 0	Laboratory: 2	Consultation: 0
Számonkérés módja v (s,v,é):				
<i>Education material</i>				
Theory				
Topic			Hét	Óra
Introduction of the safety critical software development			9.	3
Safety levels, Life cycle and development models			10.	3
Standards of the safety critical software developments			11.	3
Development environments. Risk analysis of the safety critical software development			12.	3
Laboratory				
Topic			Hét	Óra
FPGA theory, VHDL			5.	3
Development environment, logic gates in VHDL				
Full adder, data-flow and acting model			6.	3
XDC, FPGA programming				
Producing test fájl, priority encoder			7.	3
Clock generator, counter,			8.	3
Flip-flops (XDC programming)			9.	3
Komlex task: PWM signal, LED colormixing			10.	3
IP based planning			11.	3
Test work			12.	3
Free laboratory			13.	3
Demands				
Semester demands				
The code to be created jointly (with the instructor) and independently in the laboratory exercise must be uploaded by everyone in the Google classroom created for the subject, which must be accompanied by documentation.				
Homework assignments issued in labs must be uploaded to the Google classroom in the same way by the deadline. During the semester, 1 large electronic ZH dissertation is expected and 1 large homework assignment. During the semester assignments and test works, the student must achieve at least 50% of everything in order to successfully complete the semester. Method of replacement Replacement is possible at the end of the semester, once.				

<p>Method of creating the exam mark: 25% of the exam mark is given by the average of the results of the control tests, homework and reports, 25% by the test work, homework and 50% by the independent task. 0-50% insufficient, 51-65% sufficient, 66-75% medium, 76-90% good, 91-100% excellent</p>		
Literature:		
<p>Required:</p> <ol style="list-style-type: none"> 1. Sándor Tamás – Milotai Zsolt: Beágyazott rendszerek, ÓE KVK 2126, 2. Sándor Tamás, Dr. Schuster György: Informatika I., ÓE-KVK-2141, ISBN szám: 978-963-449-047-0 <p>FPGA F4modul.com/FPGA/Előadás 1a,1b,1c,1d jelzéssel ellátott diasorok.</p> <p>Könyvek:</p> <ol style="list-style-type: none"> 1. Pong P. Chu - FPGA Prototyping by VHDL Examples 2. Richard E. Haskell, Darrin M. Hanna - Digital Design Using Digilent FPGA Boards - VHDL / Active-HDL Edition 3. Enoch O. Hwang - Digital Logic and Microprocessor Design With VHDL 4. Peter J. Ashenden - The VHDL Cookbook <p>Constraint-fájl (nexys4_master.xdc): https://reference.digilentinc.com/reference/programmable-logic/nexys-4/start</p> <p>Nexys 4 board-fájlok: https://reference.digilentinc.com/learn/software/tutorials/vivado-board-files/start</p>		
<p>Ajánlott:</p> <p>Dr. Ulbert Zsolt: Szoftverfejlesztési folyamatok és szoftver minőségbiztosítás 2014 http://www.repulestudomany.hu/folyoirat/2018_1/2018-1-11-0453_Schuster_Gyorgy-Ady_Laszlo.pdf http://www.uni-obuda.hu/users/schuster.gyorgy/RTK_2018_BKS.pdf</p>		
<p>Subject quality assurance methods: The subject covers a very dynamically developing area. Therefore, the subject material should be reviewed after each academic year in consultation with industry and the material taught should be partially reworked accordingly. This basically affects the set of examples presented. Students should be involved in the examination of effectiveness and, in the event of a problem, the area in question should be reworked.</p>		