Name of the subject: **Security-critical software development**	*NEPTUN code:* KMWBS5ABNE	**Weekly hours:** 1 1 lec+ 0 gs+ 2 lab	**Credit:** 3 **Req:** Examination
Subject leader: **Dr. György Schuster**	**docent**	**Prerequsites:**	

Description of the subject:

Introduction to safety-critical software development. Safety Levels, Life Cycle and Development Model. Standards for safety-critical software development. Development environments, risks of safety critical software development.
Laboratory:
FPGA theory, VHDL basics. Development environment, Logic gates VHDL implementation. Full adder, Data flow and behaviour model. XDC, FPGA programming. Test file creation: Priority encoder, Multiplexer. Clock signal generation, division
Counting circuit. Flip-flop implementation (XDC, programming, test file creation). Using IP. IP based design. Solving a complex problem: PWM signal generation, LED colour mixing

Literature:

Pong P. Chu - FPGA Prototyping by VHDL Examples
Richard E. Haskell, Darrin M. Hanna - Digital Design Using Digilent FPGA Boards - VHDL / Active-HDL Edition
Enoch O. Hwang - Digital Logic and Microprocessor Design With VHDL
Peter J. Ashenden - The VHDL Cookbook
Constraint-fájl (nexys4_master.xdc): https://reference.digilentinc.com/reference/programmable-logic/nexys-4/start
Nexys 4 board-files:
https://reference.digilentinc.com/learn/software/tutorials/vivado-board-files/start